

II. REMARKS

Claims 1-32 are pending. One paragraph from the specification was amended to correct typographical errors. Attached hereto is Appendix A showing the changes made to the specification. No new matter has been added.

Entry of this preliminary amendment, and early consideration of this case, are respectfully requested.

Respectfully submitted,

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APPENDIX A: MARKINGS TO SHOW CHANGES MADEParagraph on page 2, lines 1-13:

In the split-gate architecture, the memory cells can be formed in mirrored pairs. Figure 1A illustrates a partially formed pair of memory cells, with floating gates 1 disposed over a substrate 2. A source region 3 is formed in the substrate 2, and is electrically connected to a source line 4. Layers of insulating materials 5 insulate floating gate 1, substrate 2, source regions 3 and source line 4 from each other. Control gates are formed by first forming a layer 6 of conductive material (such as polysilicon) over the structure, as shown in Fig. 1A. An anisotropic poly etch is then performed to remove layer 5 except for spacer portions that form the control gates, as illustrated in Fig. [2B] 1B. The problem with this configuration is that the control gate spacers 6 have sloped side wall profiles 7 that are difficult to insulate so the remaining features of the memory cells (such as drain region and electrical contacts connected thereto) can be formed. As illustrated in Fig. [3C] 1C, insulation spacers 8 can be formed against part of the sloped sidewall portion, but most of the sloped side wall portions of control gates 6 are still exposed.

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